REMARKS/ARGUMENTS

Claims 1-19 remain in the application. Claims 1, 6, 8, 14, 16, 17 and 18 are amended to more distinctly describe the subject matter of the invention. No new matter is added by these amendments.

Claims 1, 17 and 18 are amended to change the term "transaction based bus mechanism" to "transaction-based bus". The Office action notes an interpretation of "transaction based bus mechanism" that was not intended. Accordingly, it is respectfully requested that the arguments made in the Response filed on January 8, 2004 be reconsidered in view of the amendment to these claims.

A. Objection to the Drawings

The drawings were objected to as failing to show a "cache coherency transaction defined within the transaction-based bus mechanism". It is respectfully believed that Fig. 3 illustrates a generic transaction within the transaction based bus mechanism, which, in a specific instance, is a cache coherency transaction. It would not be practical or useful to illustrate each possible transaction separately. In the cache coherency transaction the responding module 309 is the central processor as noted on page 6, lines 5-8. Further, Fig. 6 shows an exemplary transaction packet that would implement the cache coherency transaction of claim 17.

As shown in Fig. 2, the cache/MMU is not coupled directly to bus 202, but instead couples through CPU 201. Hence, the drawings illustrate the feature "when the cache memory is not coupled to the transaction-based bus mechanism".

Accordingly, the illustrations are believed to be adequate.

B. Rejections under 35 U.S.C. 112.

Claims 1-8, 14, and 16-19 were rejected under 35 U.S.C. 112. This rejection is respectfully traversed.

The amendment to claim 1 is believed to overcome the objections to the terminology "the system devices" and "main memory" noted in the office action.

The amendments to claims 6, 8, 14 and 16 are believed to overcome the objection to the terminology "main memory" noted in the office action.

The amendment to claim 17 is believed to clarify that the cache coherency transaction in line 7 is the same element as referred to in lines 2-3.

C. Rejections under 35 U.S.C. 102.

Claim 17 was rejected under 35 U.S.C. 102 based upon Arimilli et al.. This rejection is respectfully traversed.

Claim 17 calls for, among other things, a computing system in which a cache coherency transaction is defined on a bus even when there is no cache memory coupled to the bus. This is not shown or suggested in the relied on reference.

Arimilli does not show or suggest a system in which there the cache is not coupled to the bus. In actuality, Arimilli teaches that the caches 56a and 56b are connected to the system bus 54. This explicitly teaches against the feature called for in claim 17 and illustrated and described in reference to Fig. 2. For at least these reasons claim 17 is not believed to be anticipated or made obvious by Arimilli.

D. Rejections under 35 U.S.C. 103.

Claims 1-4, 9-12, 18 and 19 were rejected under 35 U.S.C. 103 based upon Arimilli et al. in view of allegedly admitted prior art (AAPA). This rejection is respectfully traversed.

The AAPA is not admitted prior art. Placement of text in a section labeled "Relevant Background" does not qualify the material presented therein as prior art. Moreover, the text in that "Relevant Background" section is, unless specified otherwise, a part of the teaching of the invention, not a recitation of the prior art. Nothing in the specification, unless specified otherwise, is admitted as prior art

and it is respectfully requested that the Office supply qualified references to show any features which are allegedly supplied by the AAPA.

The rejection relies on the applicants' specification to teach that a DMA device which accesses main memory through the transaction-based bus, but does not access cache memory through the transaction-based bus. Even if the applicants' own specification was reciting prior art (which is not admitted), the recitation does not teach a DMA unit coupled to a transaction-based bus, or a system that includes a plurality of DMA-like units. Why would one include multiple DMA units?

Moreover, any rejection under 35 U.S.C. 103 requires that there be sufficient motivation to combine the teachings of the various references. This motivation must come from the prior art itself. The Office action clearly admits that the motivation to combine is provided exclusively by the alleged admitted prior art. In this manner the Office action uses Applicants' own teaching of the problems of the prior art against them. It is well settled that Applicants' own teaching cannot be used in this manner.

Accordingly, the rejection of claims 1-4, 9-12, 18 and 19 is not proper and withdrawal is respectfully requested.

Claims 5, 6, 13 and 14 were rejected under 35 U.S.C. 103 based upon Arimilli et al. in view of allegedly admitted prior art (AAPA), and further in view of Spencer. This rejection is respectfully traversed.

As noted above, the AAPA does not qualify as a reference and there is no motivation to combine the AAPA with the other references other than the motivation taught by the Applicants' themselves. Accordingly, the Office has failed to state a proper rejection of claim 5, 6, 13 and 14 and the rejection should be withdrawn.

Claims 7, 8, 15 and 16 were rejected under 35 U.S.C. 103 based upon Arimilli et al. in view of allegedly admitted prior art (AAPA), and further in view of Jacobs. This rejection is respectfully traversed.

As noted above, the AAPA does not qualify as a reference and there is no motivation to combine the AAPA with the other references other than the motivation taught by the Applicants' themselves. Accordingly, the Office has failed to state a proper rejection of claim 7, 8, 15 and 16 and the rejection should be withdrawn.

E. Conclusion.

In view of all of the above, the claims are now believed to be allowable and the case in condition for allowance which action is respectfully requested. Should the Examiner be of the opinion that a telephone conference would expedite the prosecution of this case, the Examiner is requested to contact Applicants' attorney at the telephone number listed below.

Any fee deficiency associated with this submittal may be charged to Deposit Account No. 50-1123.

Respectfully submitted,

April 26, 2004

Stuart T. Langley, Reg. No. 33,940
Hogan & Hartson LLP
One Tabor Center
1200 17th Street, Suite 1500
Denver, Colorado 80202
(720) 406-5335 Tel
(303) 899-7333 Fax